Raffar Technology Corp.

RT5957

Built-in Swift Register 8-channel PMOS with Anti-ghosting Control Function

2019/05

Version: 0.3 (Preliminary)

Description

RT5957 is an integrated 8-channel PMOS outputs with anti-ghosting function for high refresh rate LED display applications. By controlling the BK signal timeslot (LED discharge), the RT5957 is not only to prevent LED cascading bright line which caused by an LED open or short damage, but also to avoid the over reverse voltage to damage LEDs on display performance. The RT5957 gives a very simple control model to let controller determined the turn-on, discharge, and row blank timing. Built in the 8-bit shift register, RT5957 make the data transfer by serial connection without decode components on board, this also do the help on fine pitch LED display PCB layout.

The RT5957 support 2A current output for each channel.

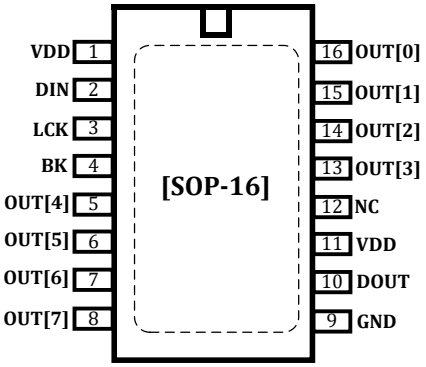
Features

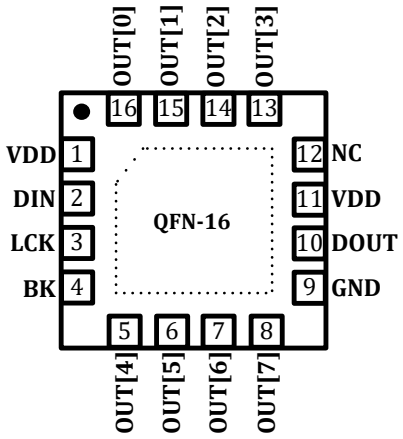
- Built-in anti-ghosting function for fine pitch LED displays
- Eliminate the LED cascading bright line caused by LED short
- Eliminate the LED cross bright line caused by LED open (along with controller)
- Serial Data connection transfer for easy and simplified PCB layout
- Wipe off 138decoder

Order Information

No.	Part No.	Package
1	RT5957SP	SOP16-150 mil-1.27 mm
2	RT5957QN	QFN16-4*4mm

Pin Assignment

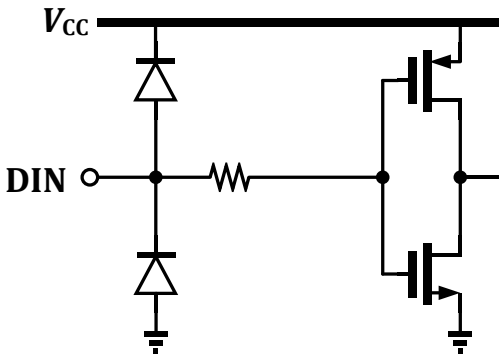




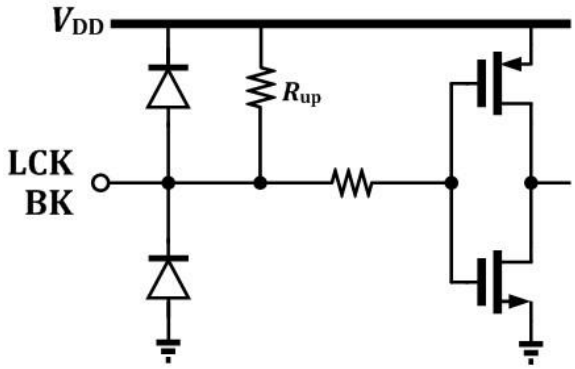
Pin No.	Pin Name	Description
1, 11	VDD	Power supply
2	DIN	Serial data input
3	LCK	Serial data strobe input
4	BK	Discharge enable control
5, 6, 7, 8, 13, 14, 15, 16,	OUT[0:7]	Current output[0:7]
9	GND	Ground
10	DOUT	Serial data output
12	NC	No connection

Input / Output Equivalent Circuits

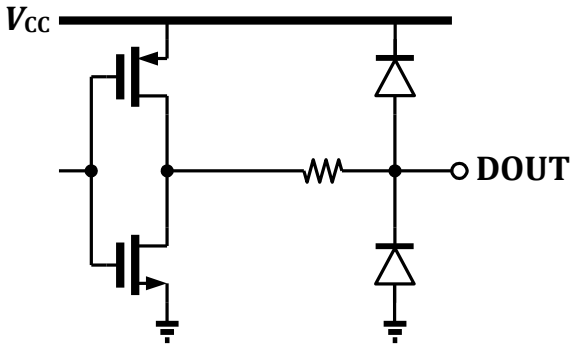
DIN



LCK, BK



DOUT



Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	0 ~ 7.0	V
Input Voltage (all pins)	V_{IN}	−0.4 ~ V_{DD} + 0.4	V
Drain Output Current	I_D	- 2.0	A
Drain Output Current (peak)	I_{DM}	-2.8	A
Power Dissipation (on 4-layer PCB)	P_D	1.6 (SOP16 · T_a = 25 °C) 2.47 (QFN16 · T_a = 25 °C)	W
Thermal Resistance (on 4-layer PCB)	$R_{th(j-a)}$	78 (SOP16) 50.6 (QFN16)	°C/W
Operating Temperature	T_{opr}	−40 ~ 85	°C
Storage Temperature	T_{stg}	−55 ~ 150	°C

*The IC reliability may be reduced when operating with the maximum rating for long periods.
*The capability of thermal dissipation is related to the dimension of thermal pad and layer numbers of the PCB.

Recommended Operating Condition

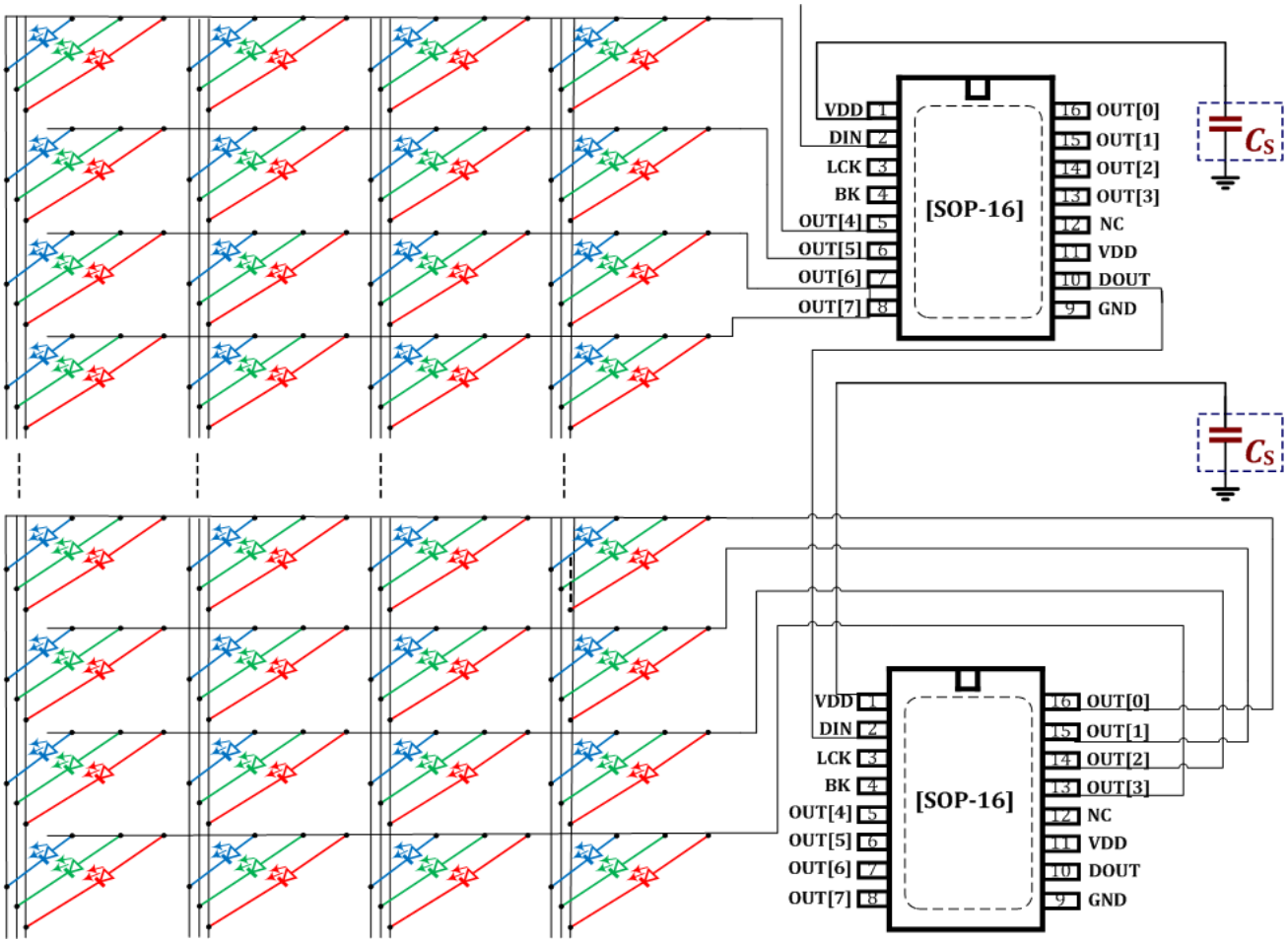
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	—	3.3	5.0	5.5	V
Output Voltage (DOUT)	V_{DOUT}	—	0.7	—	V_{DD}	V
Output Current (DOUT)	I_{OH2}	V_{OH} = V_{DD} − 0.5 V	—	−6.8	—	mA
	I_{OL2}	V_{OL} = 0.5 V	—	8.9	—	
Input Voltage (DIN, LCK, BK)	V_{IH}	V_{DD} = 3.3 V ~ 5.5 V	0.7 V_{DD}	—	V_{DD}	V
	V_{IL}		0	—	0.3 V_{DD}	

DC Electrical Characteristics (V_{DD} = 5.0 V, Ta = 25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	—	4.5	5.0	5.5	V
Output Voltage		I_{DD_OFF}	*All input keep Low*	—	62	—	uA
Gate Threshold Voltage		$V_{GS(th)}$	V_{DS}=V_{GS},I_D = -250uA	—	-0.7	-0.9	V
Drain-sourceOn-state Resistance		$R_{DS(on)[0:7]}$	V_{GS}= -5.0 V, I_D= -2.0A	—	150	200	mΩ
		$R_{DS(on)[0:7]}$	V_{GS} = -5.0 V, I_D= -1.0A	—	100	120	
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS} = -5.0V,V_{GS} = 0V	—	—	-1	uA
Input Voltage	High	V_{IH}	V_{DD} = -3.3V~5.0V	0.7 V_{DD}	—	V_{DD}	V
	Low	V_{IL}		0	—	0.3 V_{DD}	
Serial Data Output Voltage （DOUT）			I_{OH} = −6.8mA	V_{DD} – 0.5	0.5	—	
			I_{OL} = 8.9mA	—	0.5	0.8	

Recommend Application Circuit

To have the best performance of fine pitch LED display, RT5957 provides the discharge circuit to eliminate the ghosting from LED row. However, there is also a slight LED ghosting from the LED column which needs to use the LED driver with pre-charge function to achieve the non-ghosting display performance. (Pre-charge LED driver, like RT516S)



[Serial Connection]

The application note of PCB layout

To achieve the high performance of display effect and long-term stable operation, in addition to enhance the quality of module material and production processes, the PCB layout and allocation of components on board also need to put in consideration.

For module circuit design reference, below are suggested items of PCB layout:

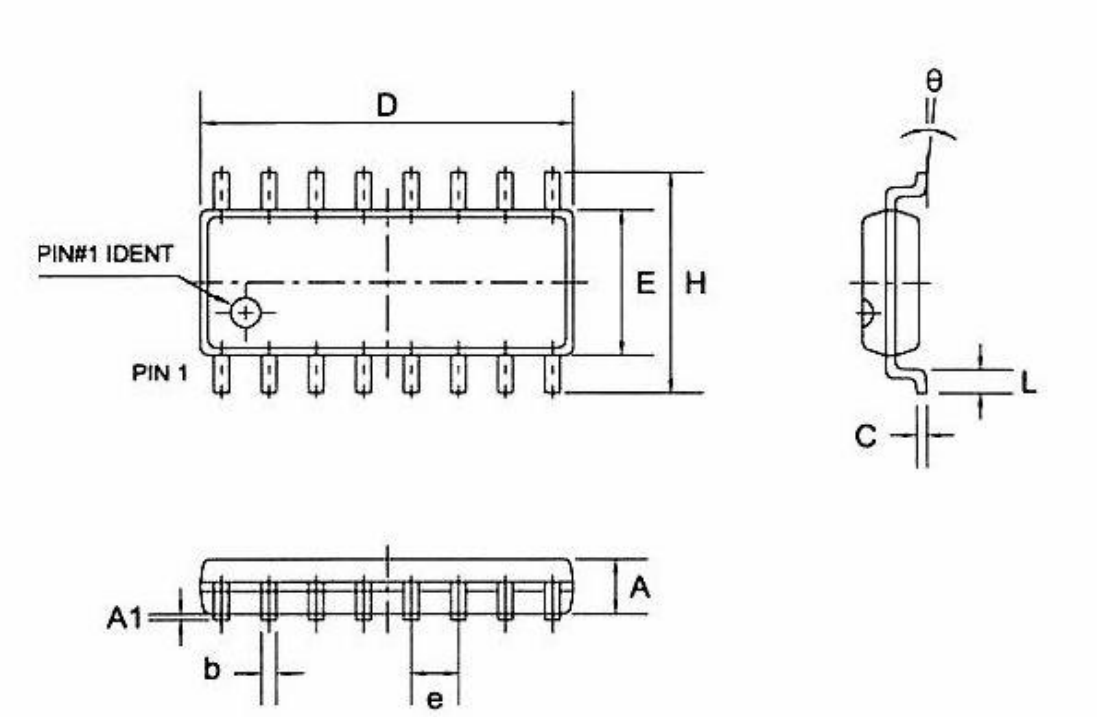
A. Strengthen the stability of power signal:
   During the operation, the outputs of RT5957 continuously switch with high current and this leads the VDD signal becomes more severe vibration and decrease the average voltage level. Therefore, suggest to widening the RT5957 VDD signal path or adding multi path of VDD, also put the by-pass capacitor, Cs (1uF), as close as possible to the VDD pins to enhance the stability of power signal.

B. Isolate the noise interference of input signal:
   The signal path of DIN, LCK and BK of RT5957 is suggested to be isolated from the high frequency signal path, such as clock, latch or OE pins of other constant current ICs. The ideal design is to make the DIN, LCK and BK of RT5957 with independent path and to be isolated by GND path.

C. Optimize the 245 output signal:
   Use can choose the 245 chip with higher drive capability and stability (e.g. NXP 74HC245) to improve the adaptability of operating in high frequency noise conditions;
   Suggest one 245 output is not over 8~10 RT5957 LCK or BK signal in parallel to lower the voltage insufficient / phase delay caused by load effect;
   In addition, if the number of 245 output channels is sufficient, suggest planning to use one 245 chip only for RT5957 input signal, DIN, LCK and BK.

Package Outline

SOP16 (150mil, 1.27mm)

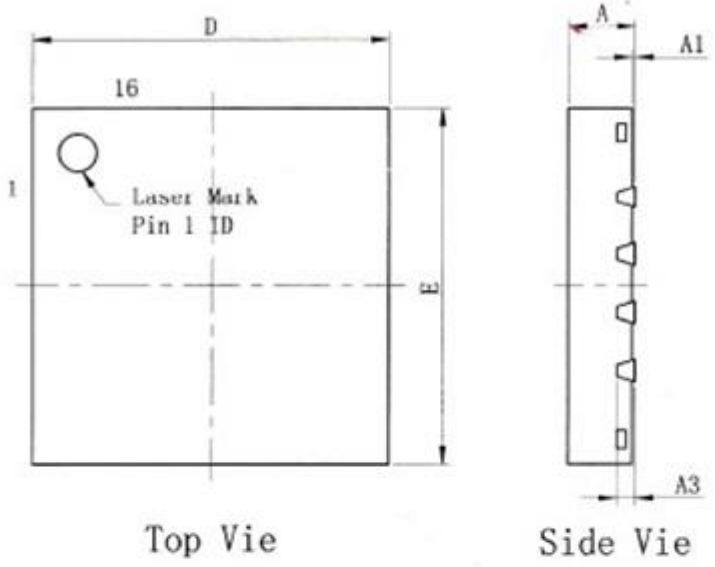


Symbol	Millimeter (mm)		Inch (in)	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.102	0.254	0.004	0.010
b	0.300	0.550	0.012	0.022
C	0.150	0.350	0.006	0.014
D	9.700	10.30	0.382	0.406
E	3.750	4.150	0.148	0.163
H	5.800	6.200	0.228	0.244
e	1.27 (BSC)		0.050 (BSC)	
L	0.450	0.850	0.018	0.033
θ°	0	8	0	8

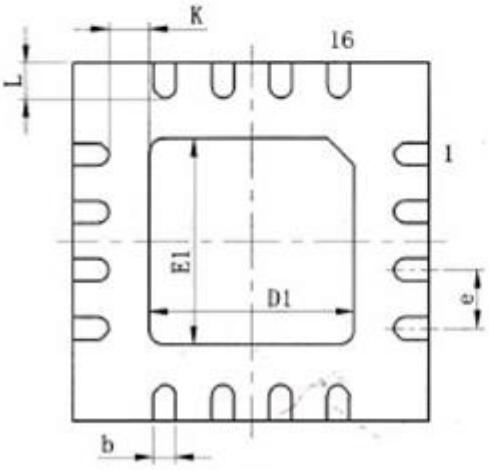
QFN16 (4x4 mm)

Dimension: mm

Symbol	Min.	Std.	Max.	Symbol	Min.	Std.	Max.
A	0.70	0.75	0.80	D1	2.20	2.30	2.40
A1	0.00	--	0.05	E1	2.20	2.30	2.40
A3	0.203REF			E	0.65TYP		
b	0.20	0.25	0.30	K	0.20	-	-
D	3.90	4.00	4.10	L	0.30	0.40	0.50
E	3.90	4.00	4.10				



Top Vie Side Vie



Bottom Vie

Note

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