Raffar Technology Corp.

RT5960

Built-in Shift Register 16-channel PMOS with Anti-ghosting Control Function

2016/11

Version: 0.2 (Preliminary)

Description

RT5960 is a 16-channel PMOS for high refresh rate LED display application. By controlling the BK signal timeslot (LED discharge), the RT5960can effectively to eliminate the LED ghosting phenomena , to prevent LED cascading blink which caused by a LED open or short damage, and also to avoid the over reverse voltage to damage LEDs on display performance. The RT5960 gives a very simple control model to let controller determined the turn-on, discharge, and row blank timing. Built-in the 16-bit shift register, RT5960 makes the data transfer by serial connection without decoding component on board to simplify the PCB layout.

The RT5960 support 2A current output for each channel.

Features

- Built-in anti-ghosting function (last scan ghost image) for dynamic LED display
- Eliminate the LED cascading blink caused by LED short.
- Eliminate the LED cross blink caused by LED open
- Serial Data connection transfer for easy and simplified PCB layout
- Wipe off 138decoder
- High speed switch application
- Extra low $R_{DS(on)}$

  $R_{DS(ON)}$, V_{gs}@-5.0V,I_{ds}@-1.0A ≤ 90mΩ

  $R_{DS(ON)}$, V_{gs}@-5.0V,I_{ds}@-2.0A ≤ 120mΩ

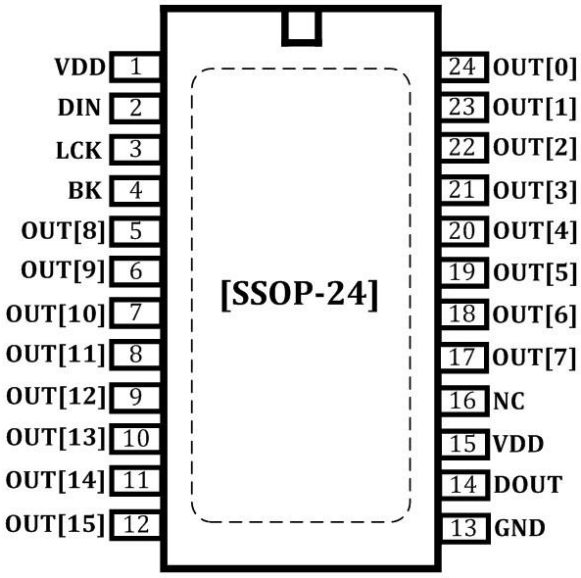
Application

Indoor and outdoor LED display

Order Information

No.	Part No.	Package
1	RT5960SS	SOP24-150 mil-0.635 mm

Pin Assignment

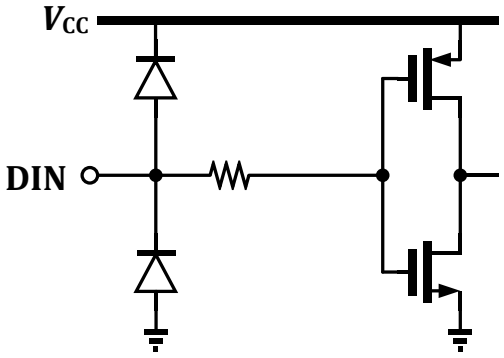


Pin Description

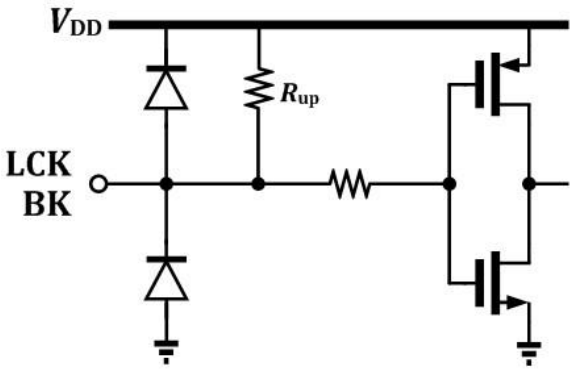
Pin No.	Pin Name	Description
1, 15	VDD	Supply voltage (both pins have to be connected to power)
2	DIN	Serial data input
3	LCK	Serial data strobe input
4	BK	Discharge enable control
5, 6, 7, 8, 9,10,11 12, 17,18, 19,20,21 22,23,24	OUT[0:15]	Current output[0:15]
13	GND	Ground
14	DOUT	Serial data output
16	NC	No connection

Input/output Equivalent Circuits

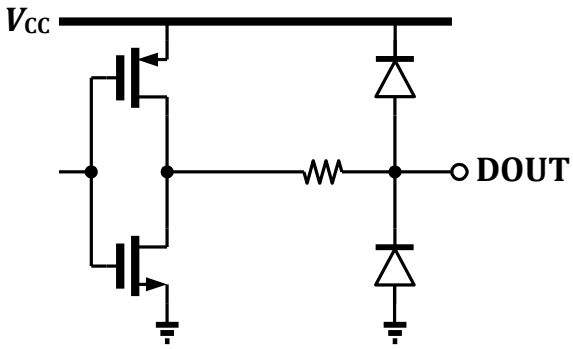
DIN



LCK, BK



DOUT



Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	0 ~ 7.0	V
Input Voltage (all pins)	V_{IN}	−0.4 ~ V_{DD} + 0.4	V
Drain Output Current	I_D	- 2.0	A
Drain Output Current (peak)	I_{DM}	-2.8	A
Power Dissipation (on 4-layer PCB)	P_{D_max}	1.67 (SSOP-24 · T_a = 25°C)	W
Thermal Resistance (on 4-layer PCB)	$R_{th(j-a)}$	75 (SSOP-24)	°C/W
Operating Temperature	T_{opr}	−40 ~ 85	°C
Storage Temperature	T_{stg}	−55 ~ 150	°C

Recommended Operating Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	—	3.3	5.0	5.5	V
Output Voltage (DOUT)	V_{DOUT}	—	0.7	—	V_{DD}	V
Output Current (DOUT)	I_{OH2}	V_{OH} = V_{DD} − 0.5 V	—	6.8	—	mA
	I_{OL2}	V_{OL} = 0.5 V	—	8.9	—	
Input Voltage (DIN, LCK, BK)	V_{IH}	V_{DD} = 3.3 V ~ 5.5 V	0.7 V_{DD}	—	V_{DD}	V
	V_{IL}		0	—	0.3 V_{DD}	

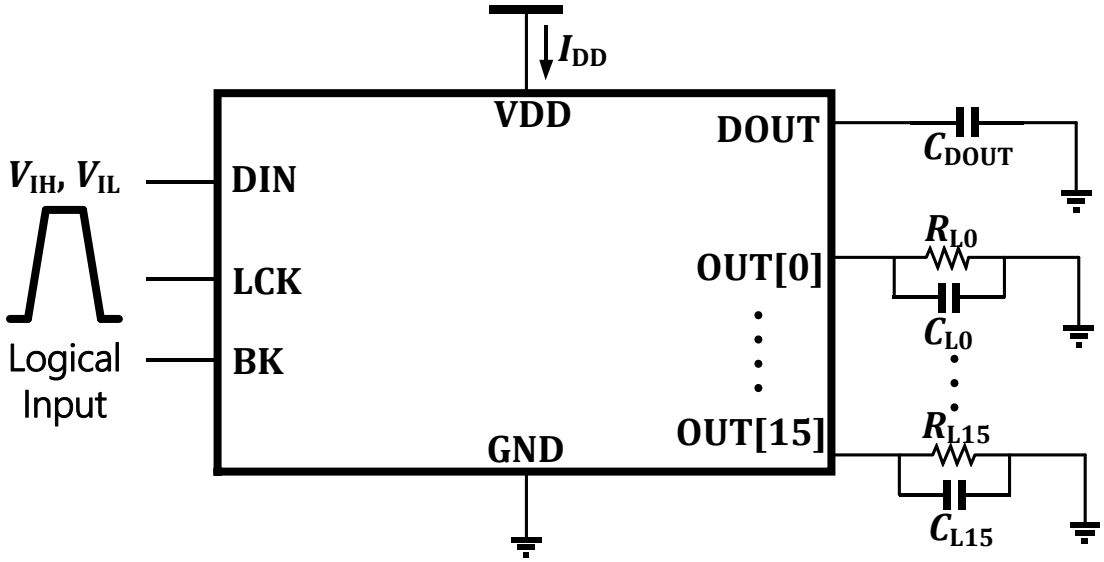
DC Electrical Characteristics (V_{DD} = 5.0 V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	—	4.5	5.0	5.5	V
Output Voltage		I_{DD_OFF}	*All input keep Low*	—	66	—	uA
Gate Threshold Voltage		$V_{GS(th)}$	V_{DS}=V_{GS},I_D = -250uA	—	-0.7	-0.9	V
Drain-sourceOn-state Resistance		$R_{DS(on)[0:15]}$	V_{GS}= -5.0 V, I_D= -2.0A	—	90	—	mΩ
		$R_{DS(on)[0:15]}$	V_{GS} = -5.0 V, I_D= -1.0A	—	75	—	
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS} = -5.0V,V_{GS} = 0V	—	—	-1	uA
Input Voltage	High	V_{IH}	V_{DD} = 3.3V~5.0V	0.7 V_{DD}	—	V_{DD}	V
	Low	V_{IL}		0	—	0.3 V_{DD}	
Serial Data Output Voltage （DOUT）		I_{DSS}	I_{OH} = −6.8mA	V_{DD} − 0.5	0.5	—	
			I_{OL} = 8.9mA	—	0.5	0.8	

Switching Characteristics (V_{DD} = 5.0 V)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Current Delay Time On, (VOUT[0:15])	$T_{D(ON)}$	V_{DD} = 5.0V I_D = -1A $R_{L[0:15]}$ = 5Ω $C_{L[0:15]}$= 12pF C_{DOUT}= 12pF	—	12.1	—	ns
Output Current Rise Time (VOUT[0:15])	T_r		—	63.5	—	
Output Current Delay Time Off, (VOUT[0:15])	$T_{D(OFF)}$		—	22.7	—	
Output Current Fall Time (VOUT[0:15])	T_f		—	5.17	—	

[Dynamic Test]

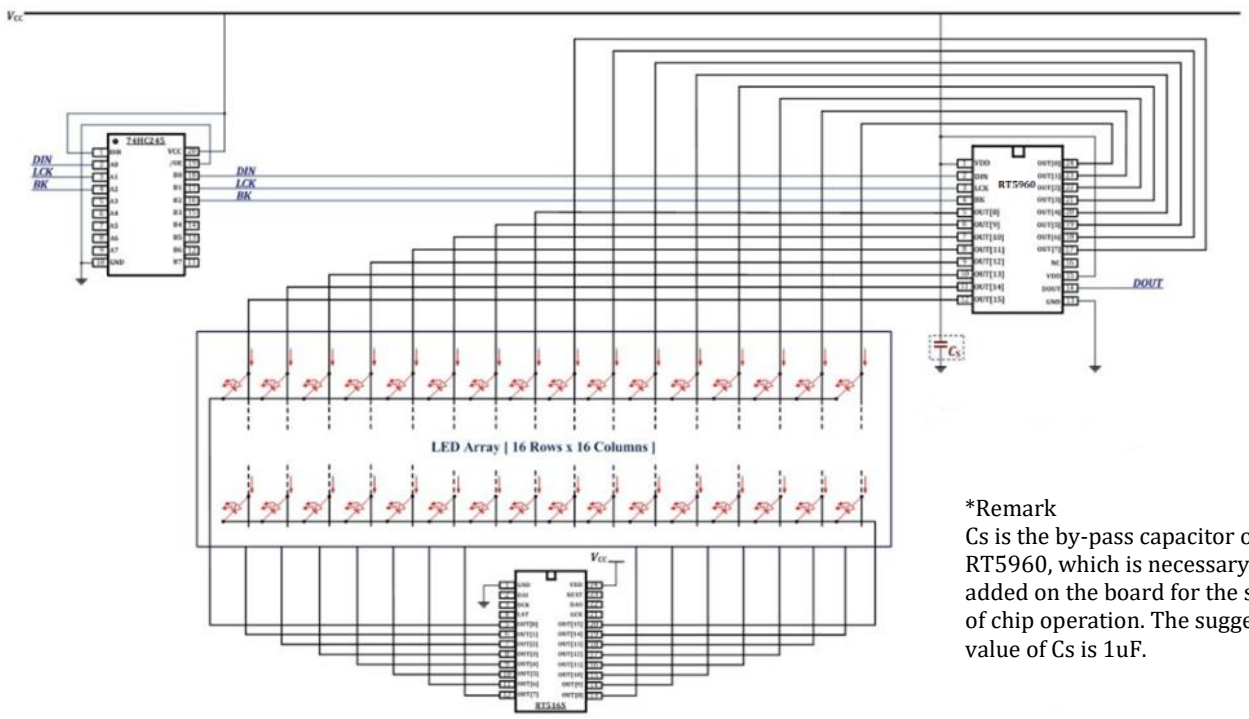


Recommend Application Circuit

To have the best performance of fine pitch dynamic LED display, RT5960 provides the discharge circuit to eliminate the ghosting from LED row. However, there is also a slight LED ghosting from the LED column which needs to use the LED driver with pre-charge (e.g. RT516S) function to achieve the non-ghosting display performance.

By controlling the BK signal timeslot (LED discharge), the RT5960 can effectively avoid the over reverse voltage to damage LEDs and prevent LED cascading blink caused by a LED open or short.

RT5960 is an integrated 16 outputs PMOS. To avoid the thermal issue, RT5960 is suggested to use for an over (>) 32 scan display application and the IC temperature has to be monitored in practical use.



*Remark
Cs is the by-pass capacitor of RT5960, which is necessary to be added on the board for the stability of chip operation. The suggested value of Cs is 1uF.

【Typical 16-scan application circuit】

The application note of PCB layout

To achieve the high performance of display effect and long-term stable operation, in addition to enhance the quality of module material and production processes, the PCB layout and allocation of components on board also need to put in consideration.

For module circuit design reference, below are suggested items of PCB layout:

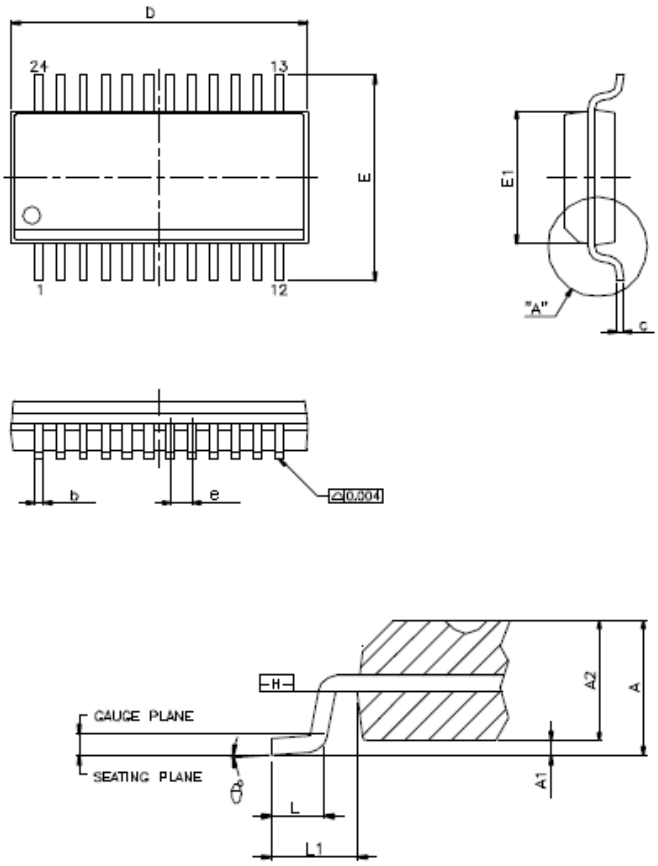
A. Strengthen the stability of power signal:
   During the operation, the outputs ofRT5960 continuously switch with high current and this leads the VDD signal becomes more severe vibration and decrease the average voltage level. Therefore, suggest to widening the RT5960 VDD signal path or adding multi path of VDD, also put the by-pass capacitor, Cs (1uF), as close as possible to the VDD pins to enhance the stability of power signal.

B. Isolate the noise interference of input signal:
   The signal path of DIN, LCK and BK of RT5960 is suggested to be isolated from the high frequency signal path, such as clock, latch or OE pins of other constant current ICs. The ideal design is to make the DIN, LCK and BK of RT5960 with independent path and to be isolated by GND path.

C. Optimize the 245 output signal:
   Use can choose the 245 chip with higher drive capability and stability (e.g. NXP 74HC245) to improve the adaptability of operating in high frequency noise conditions;
   Suggest one 245 output is not over 8~10 RT5960 LCK or BK signal in parallel to lower the voltage insufficient / phase delay caused by load effect;
   In addition, if the number of245 output channels is sufficient, suggest planning to use one 245 chip only for RT5960 input signal, DIN, LCK and BK.

Package Outline

SOP24 Dimension (150mil, 0.635mm)



Symbol	Millimeter (mm)		Inch (in)	
	Min.	Max.	Min.	Max.
A	1.346	1.753	0.053	0.069
A1	0.102	0.254	0.004	0.010
A2	-	1.499	-	0.059
b	0.203	0.305	0.008	0.012
C	0.178	0.254	0.007	0.010
D	8.560	8.738	0.337	0.344
E	5.791	6.198	0.228	0.244
e	0.635 (BSC)		0.025 (BSC)	
E1	3.810	3.998	0.150	0.157
L	0.406	1.270	0.016	0.050
L1	1.041 (BSC)		0.0409 (BSC)	
θ°	0	8	0	8

Note

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